DEENBANDHU CHHOTU RAM UNIVERSITY OF SCIENCE & TECHNOLOGY, MURTHAL (SONEPAT)
SCHEME OF STUDIES AND EXAMINATION
B. TECH. II YEAR (ELECTRONICS & COMMUNICATION ENGINEERING)
SEMESTER III
Credit Based Scheme w.e.f. 2013-2014

Sr. No.	Course No.	Course Title	Teaching Schedule			Marks of Class Work	Exam. Marks		Total Marks	Credit	Duration of Exam
			L	T	P		Theory	Practical			
1	MGT201B	ENGINEERING ECONOMICS **(Common for all branches Except BT& BME) (Gr-A)**	4	-	-	25	75	-	100	4	3
	OR										
	GES201B	ENVIRONMENTAL STUDIES**(Common for all branches) (Gr-B)**	3	-	-	-	75	-	75	-	3
2	ECE201B	DIGITAL ELECTRONICS(EE, ECE, CSE,IC,EEE,common with BME,AEI in 4th Sem.)	3	1	-	25	75	-	100	4	3
3	EE211B	NETWORK ANALYSIS AND SYNTHESIS (ECE,AEI)	3	1	-	25	75	-	100	4	3
4	ECE203B	ANALOG ELECTRONICS (BME,ECE,common with 4TH Sem. AEI)	3	1	-	25	75	-	100	4	3
5	ECE207B	SIGNALS & SYSTEMS	3	1	-	25	75	-	100	4	3
6	CSE201B	DATA STRUCTURES (CSE,ECE,AEI)	3	1	-	25	75	-	100	4	3
7	ECE221B	DIGITAL ELECTRONICS LAB (EE, ECE, CSE,IC,EEE,common with BME,AEI in 4th Sem.)	-	-	2	20	-	30	50	1	3
8	ECE223B	ANALOG ELECTRONICS LAB (BME,ECE, common with 4th Sem. AEI)	-	-	2	20	-	30	50	1	3
9	EE241B	NETWORK ANALYSIS AND SYNTHESIS LAB(ECE,AEI)	-	-	2	20	-	30	50	1	3
10	CSE221B	DATA STRUCTURES LAB (CSE,ECE,AEI)	-	-	2	20	-	30	50	1	3
11	GES203B	ENVIRONMENTAL STUDIES FIELD WORK**(Gr-B)**	-	-	-	-	-	25	25	-	-
12	ME217B	WORKSHOP TRAINING **(Common for all branches Except BT & AE)**	-	-	2	50	-	-	50	2	-
Total		**Gr-B**	**18**	**5**	**10**	**255**	**375**	**120**	**750**	**26**	
		Gr-A	**19**	**5**	**10**	**280**	**450**	**120**	**850**	**30**	

Note:

1. Every student has to participate in the sports activities. Minimum one hour is fixed for sports activities either in the morning or evening. Weightage of Sports is given in General Proficiency Syllabus.
2. The students will be allowed to use non-Programmable Scientific Calculator. However, sharing/exchange of calculator is prohibited in the examination.
3. Electronic Gadgets including Cellular Phones are not allowed in the examination.
4. Assessment of Workshop Training (ME217B) will be based on seminar, viva-voce, report and certificate of professional training obtained by the student from in-house workshop.
5. All the branches are to be divided into group 'A' and 'B' as per the suitability of the institute/college, so that there is an equitable distribution of teaching load in odd and even semesters.

Subject to be taught to other departments which are not in above scheme

Sr. No.	Course No.	Course Title	Teaching Schedule			Marks of Class Work	Exam. Marks		Total Marks	Credit	Duration of Exam
			L	T	P		Theory	Practical			
1	ECE205B	ELECTRONICS ENGINEERING (CHE)	3	1	-	25	75	-	100	4	3
2	ECE210B	COMMUNICATION SYSTEMS (CSE)	3	1	-	25	75	-	100	4	3
3	ECE225B	ELECTRONICS ENGINEERING LAB(CHE)	-	-	2	20	-	30	50	1	3

B. Tech. Semester – III (Common for all Branches Except BT& BME)

L	T	P	Credits
4	-	-	4

Class Work	:	25 Marks
Theory	:	75 Marks
Total	:	100 Marks

Duration of Exam. : 3 Hrs.

UNIT I

Definition of economics: Various definitions, nature of Economic problem, Micro and macro economics- their feature and scope, production possibility curve, Economic laws and their nature. Relation between Science, Engineering Technology and Economics. Concept and measurement of utility, Law of Diminishing Marginal Utility, Law of equi-marginal utility – its practical application and importance**.**

UNIT II

Meaning of Demand, Individual and Market demand schedule, Law of demand, shape of demand curve. Elasticity of demand, measurement of elasticity of demand, factors effecting elasticity of demand, practical importance & application of the concept of elasticity of demand. Various concepts of cost-Fixed cost, variable cost, average cost, marginal cost, money cost, real cost, opportunity cost. Shape of average cost, marginal cost, total cost etc. in short run and long run.

UNIT III

Meaning of production and factors of production; Law of variable proportions, Law of Return to Scale, Internet and External economics and diseconomies of scale. Meaning of Market, Type of Marker– perfect Competition, Monopoly, Oligopoly, Monopolistic competition (Main features of these markers).

UNIT IV

Supply and Law of Supply, Role of Demand & Supply in Price Determination and effect of changes in demand and supply on prices . Nature and characteristics of Indian economy, privatization – meaning, merits and demerits. Globalisation of India economy – merits and demerits. Elementary Concept of WTO & TRIPS agreement, Monitory Policy & Fiscal Policy.

Text Books:

1. Ahuja H.L"Micro Ecomomic Theory" S. Chand Publication, New Delhi
2. Dewett K.K "Modern Ecomomic Theory" S. Chand Publication, New Delhi
3. Jain T.R, Grover M.L, Ohri V.K Khanna O.P,"Economics for engineers" V.K .Publication ,New Delhi

Reference Books:

1. Jhingan M.L"Micro Ecomomic Theory" S.Chand Publication ,New Delhi
2. Chopra P.N "Principle of Economics" Kalyani Publishers, Delhi
3. Mishra S.K "Modern Micro Economics" Pragati Publication Mumbai.
4. Dwivedi D.N "Micro Economics " Pearson Education, New Delhi.

NOTE:

1. In the Semester examination, the examiner will set 08 questions in all selecting two from each unit. The candidates will be required to attempt five questions in all, atleast one from each unit. All questions carry equal marks.
2. The students will be allowed to use non-Programmable Scientific Calculator. However, sharing/exchange of calculator are prohibited in the examination.

ECE201B DIGITAL ELECTRONICS

B. Tech. Semester –III (EE, ECE, CSE, EEE, IC, common with BME, AEI in 4th Sem.)

L	T	P	Credits
3	1	-	4

Class Work	:	25 Marks
Theory	:	75 Marks
Total	:	100 Marks

Duration of Exam. : 3 Hrs.

UNIT I

FUNDAMENTALS OF DIGITAL TECHNIQUES :
Digital signal, logic gates: AND, OR, NOT, NAND, NOR, EX-OR, EX-NOR, Boolean algebra. Review of Number systems. Binary codes: BCD, Excess-3, Gray, EBCDIC, ASCII, Error detection and correction codes.
COMBINATIONAL DESIGN USING GATES:
Design using gates, Simplifications of SOP and POS Boolean Expressions, Karnaugh map up to four variables.

UNIT II

COMBINATIONAL DESIGN USING MSI DEVICES :
Multiplexers and Demultiplexers and their use as logic elements, Decoders, Adders / Subtractors, BCD arithmetic circuits, Encoders, Code Converters, Decoders / Drivers for display devices.
SEQUENTIAL CIRCUITS:
Flip Flops : S-R, J-K, T, D, master-slave, edge triggered, shift registers, sequence generators, Counters, Asynchronous and Synchronous Ring counters and Johnson Counter, Design of Synchronous and Asynchronous sequential circuits.

UNIT III

DIGITAL LOGIC FAMILIES:
Switching mode operation of p-n junction, bipolar and MOS. devices. Bipolar logic families:RTL, DTL, DCTL, HTL, TTL, ECL, MOS, and CMOS logic families. Tristate logic, Interfacing of CMOS and TTL families.
SEMICONDUCTERS MEMORY DEVICES:
Memory organizations, Characteristics of memory devices, Classifications of semiconductors memories.

UNIT IV

A/D AND D/A CONVERTERS:
Sample and hold circuit, weighted resistor and R -2 R ladder D/A Converters, specifications for D/A converters.
A/D converters : Quantization, parallel -comparator, successive approximation, counting type, dual-slope ADC, specifications of ADCs.
PROGRAMMABLE LOGIC DEVICES:
PLA, PAL, FPGA and CPLDs.

Text Books :
1. Modern Digital Electronics(Edition III) : R. P. Jain; TMH
2. Digital Electronics :Green; Pearson

Reference Books:
1. Digital Integrated Electronics : Taub & Schilling; MGH
2. Digital Principles and Applications : Malvino & Leach; McGraw Hill.
3. Digital Design : Morris Mano; PHI.

NOTE:
In the Semester examination, the examiner will set 08 questions in all selecting two from each unit. The candidates will be required to attempt five questions in all, atleast one from each unit. All questions carry equal marks.

Approved by UG BOS & FET

EE211B **NETWORK ANALYSIS & SYNTHESIS**

B. Tech. Semester –III (ECE, AEI)

L	T	P	Credits
3	1	-	4

Class Work	:	25 Marks
Theory	:	75 Marks
Total	:	100 Marks

Duration of Exam. : 3 Hrs.

UNIT I

TRANSIENT RESPONSE:
Laplace Transform: Review of properties and applications of Laplace transform of complex waveform. Transient Response of RC, RL, RLC series, parallel, series-parallel circuits to various excitation signals such as step, ramp, impulse and sinusoidal excitations using Laplace transform.

UNIT II

TWO-PORT NETWORKS:
Characteristics and parameters of two port networks**,** Network Configurations**,** short-circuit Admittance parameters, open-circuit impedance parameters, Transmission parameters, hybrid parameters, condition for reciprocity & symmetry of two-port networks in different parameters representations. Inter-relationships between parameters of two-port network sets, Inter-connection of two port networks.

UNIT III

FILTERS:
Filter fundamentals, classification of Filter, Analysis & design of prototype high-pass, prototype low-pass, prototype band-pass, and prototype band-reject Filter, m-derived low-pass & high-pass filters.
TOPOLOGY: Principles of network topology, graph matrices, network analysis using graph theory

UNIT IV

NETWORK SYNTHESIS:
Network functions, concept of poles and zeros in Network functions, Time domain behavior from the pole-zero plot., Hurwitz polynomials**,** Positive real functions, procedure of testing of PR functions, concept and procedure of network synthesis, properties of expressions of driving point immitances of LC networks. LC Network synthesis: Foster's I & II Form, Cauer's I & II form.

TEXT BOOKS:

1. Network Theory Analysis & Synthesis: Smarajit Ghosh; PHI.
2. Network Analysis & Synthesis: F.F.Kuo; John Wiley & Sons Inc.

REFERENCE BOOKS:

1. Introduction to modern Network Synthesis: Van Valkenburg; John Wiley
2. Network Analysis: Van Valkenburg; PHI
3. Basic circuit theory:Dasoer Kuh; McGraw Hill.
4. A Course in Electrical Circuit Analysis by Soni & Gupta; Dhanpat Rai Publication.
5. Circuit Analysis: G.K. Mithal; Khanna Publication.
6. Networks and Systems: D.Roy Choudhury; New Age International
7. Engineering Circuit Analysis; Hayat & Kemmerley TMH.

NOTE:
In the Semester examination, the examiner will set 08 questions in all selecting two from each unit. The candidates will be required to attempt five questions in all, atleast one from each unit. All questions carry equal marks.

Approved by UG BOS & FET

ECE203B **ANALOG ELECTRONICS**

B. Tech. Semester –III (BME, ECE, common with 4th Sem. AEI)

L	T	P	Credits
3	1	-	4

Class Work	:	25 Marks
Theory	:	75 Marks
Total	:	100 Marks

Duration of Exam. : 3 Hrs.

UNIT I

BASIC SEMICONDUCTOR AND PN-JUNCTION THEORY:
Introduction, Atomic Structure, Covalent Bond, Metals, Insulators & Semiconductors, Effect of Temperature on Conduction, Drift Current ,Donor & Accepter Impurities in Semiconductor, Law Of Mass Action, Hall's Effect, Hall Coefficient & Mobility, Numerical.

CHARACTERISTICS OF DIODE:
PN-Junction, Construction Types, Unbiased Junction, Biased Junction, Space Charge Region, Diode Characteristics & Parameters, Diode Capacitance, Diode Resistance, DC And AC Load Lines, Diode Testing, Zener And Avalanche Breakdown Diodes, Tunnel Diode, Temperature Characteristics of Diode, Reverse Recovery Time, Switching Characteristics of Diode.

UNIT II

DIODE APPLICATIONS:
Half Wave, Full Wave Center Tapped, Full Wave Bridge(Rectification), Series Clipping Circuit, Shunt Clipping Circuit, Clamping Circuit, Bridge Voltage Doubler, Filtering Circuit Using Capacitor & Inductor.

JUNCTION TRANSISTOR:
Introduction, Construction Of Junction Transistor, Circuit Symbols, Transistor Operation, Unbiased Transistor, Operation Of Biased Transistor, Transistor Current Components, DC & AC Load Line, Operating Point, Transistor Configuration CB, CE, CC, Input/Output Characteristics, Early Effect(Base Width Modulation), Eber's-Moll-Model of Transistor, Maximum Rating of Transistor, Transistor Testing, Transistor as an Amplifier, Transistor as Oscillator.

UNIT III

BJT BIASING:
Bias Stability, Instability Due To β, Thermal Stability, Stability Factor, Fixed Biased Circuits, Effect of Emitter Resistor, Collector to Base Bias, Voltage Divide Biasing, Advantage & drawbacks of Biasing Techniques, Stability Factor calculation of Biasing Techniques, Bias Compensation by various device, Thermal Runway, Transistor Dissipation, Thermal Resistance, Condition of Thermal Stability

SMALL SIGNAL CIRCUIT:
Two Port Network, Hybrid(H-Parameter)Model, Typical Values of H-Parameter Model, Conversion of CE, CB, CC Configuration to Equivalent Hybrid Model, CB Circuit Analysis, CE circuit with & without R_E analysis, CC circuit analysis, Analysis of CE, CB & CC Configuration with approximate Hybrid Model, Miller's Theorem, Dual of Miller Theorem.

UNIT IV

HIGH FREQUANCY ANALYSIS:
Hybrid Pi Model, CE Short Circuit Gain, Frequency Response, Alpha Cut off Frequency, Gain Bandwidth Product, Emitter Follower at High Frequencies.

FET:
Introduction, The Junction FET, Basic Construction, Operation, P- Channel FET, N-Channel FET, High Frequency Model of FET, Low Frequency FET Amplifiers, Transfer Characteristics of FET, MOSFET, Enhancement Mode, Depletion Mode of FET, Circuit Symbol of MOSFET,V-MOSFET.

Reference Books:

1. Basic Electronics By Debashion DE. -- Pearson.
2. Electronics Device & Circuit, By Robert Boylestad ,Louis Nashelsky.
3. Electronics Device Circuit By David.A.Bell -- Oxford
4. Integrated Electronics By Millman Halkias -- TMH.
5. Electronics Device &Circuit By Dharam Raj Cheruku -- Pearson.

NOTE:
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Approved by UG BOS & FET

ECE207B **SIGNALS & SYSTEMS**

B. Tech. Semester –III

L	T	P	Credits
3	1	-	4

Class Work	:	25 Marks
Theory	:	75 Marks
Total	:	100 Marks

Duration of Exam. : 3 Hrs.

UNIT I

INTRODUCTION TO SIGNAL:

Signal Definition, Classification with examples: Continuous –Time & Discrete –Time, Continuous –valued & Discrete –valued, Analog & Digital, Deterministic & Random, One Dimensional & Multi Dimensional, Single-channel & Multi Channel, Even/Symmetric & Odd/Anti symmetric signals, Causal, Non causal & Anti causal; Real & Complex, Periodic & Aperiodic, Energy & Power signals; Representation of Discrete –Time signals, Elementary Discrete Time Signals.

INTRODUCTION TO SIGNAL PROCESSING:

Design Signal Processing, Analog Signal Processing (ASP), Digital Signal Processing (DSP), Comparison of ASP & DSP, Discrete –Time Processing of Continuous –Time Signals, Basic Sampling & Reconstruction Theorem, Effect of Under sampling: Aliasing.

UNIT II

INTRODUCTION TO DISCRETE-TIME SYSTEM AND THEIR PROPERTIES:

Systems & Their Representation, Independent variable transformations: Time Shifting, Time Reversal, Time Scaling; classification of Systems: Hardware, Software & Mixed Systems; Linear & Nonlinear Systems; Static/without memory & Dynamic/ with memory Systems, Causal & Noncausal System; Invertible & Noninvertible; Stable & Unstable System, Time variant & Time Invariant Systems.

LINEAR-TIME INVARIENT(LTI) SYSTEMS AND THEIR ADVANTAGES:

Linear Time-Invariant Systems, Discrete –time Signal representation in terms of impulses, Impulse Response of Discrete Time LTI Systems, Finite Impulse Response System, Infinite Impulse Response System, LTI Systems Properties, LTI systems representation by Constant – Coefficient Difference Equation, Block Diagram Representation of First order systems described by difference equations, LTI System Characterization, Cascade & Parallel Connection of LTI Systems.

UNIT III

FOURIER SERIES REPRESENTATION FOR PERIODIC SIGNALS:

Introduction to Frequency domain Representation, Concept of frequency for analog signals and discrete –time signals, Fourier Series Representation of Periodic Signals, Convergence of the Fourier Series, Properties of Discrete-Time Fourier Series, I/P O/P Relationship for LTI Systems using Fourier Series, Filtering Concept.

DISCRETE-TIME FOURIER TRANSFORM:

Fourier Transform representation for Discrete –Time Aperiodic & Periodic Signals, Properties of Discrete –Time Fourier Transform, Basic Fourier Transform Pairs, Duality Between Time & Frequency Domains, Systems Characterized by Linear Constant Coefficient Difference Equations.

UNIT IV

Z-TRANSFORM AND ITS INVERSE:

Introduction to Z-Transform, Region of Convergence (ROC) for Z-Transform, ROC for: Finite & Infinite Duration; Causal, Anti causal & Noncausal signals; Z-Transform Properties, Inverse Z-Transform By: Contour integration, Power series expansion, Partial –Fraction Expansion, Common Z-Transform Pairs, Rational Z –Transforms: Poles & Zeros of Signals & Systems, Pole Location and Time Domain behaviour for Causal Signals.

APPLICATION OF Z-TRANSFORM:

System Function of an LTI System, Response of LTI System with Rational System Functions, Transient & Steady –State Responses, Causality & Stability of LTI Systems, Pole Zero Cancellation.

Text Books:

1. A. V. Oppenheim, A. S. Willsky, with S. Nawab “Signals & Systems”, Prentice –Hall India.
2. Ghosh,”Signal & Systems”,Pearson.
3. Nagrath & R. Ranjan, “Signals & Systems”, TMH.

Reference Books:

1. S. Salivahanan, A. Vallavraj, C. Gnanapriya, “ Digital Signal Processing”, Tata McGraw Hill.
2. J. G. Proakis, D. G. Manolakis, “Digital Signal Processing, Principles, Algorithms, & Applications”, Prentice –Hall India.
3. Haykin, Van Veen,”Signal & Systems”,Wiley.
4. Schaum Series, “Signals & Systems”,Sue & Ranjan.

NOTE:

In the Semester examination, the examiner will set 08 questions in all selecting two from each unit. The candidates will be required to attempt five questions in all, atleast one from each unit. All questions carry equal marks.

Approved by UG BOS & FET

CSE201B **DATA STRUCTURES**

B. Tech. Semester –III (CSE, ECE, AEI)

L	T	P	Credits
3	1	-	4

Class Work	:	25 Marks
Theory	:	75 Marks
Total	:	100 Marks

Duration of Exam. : 3 Hrs.

UNIT I

Basic Terminology: Elementary Data Organization, Data Structure Operations.
Arrays: Array Definition and Analysis, Representation of Linear Arrays in Memory, Traversing of Linear Arrays, Insertion and Deletion, Single Dimensional Arrays, Two Dimensional Arrays, Multidimensional Arrays, Sparse Matrix.
Stacks and Queues: Operations on Stacks- Push, Pop, Peep, Representation of stacks. Application of stacks - polish expression and their compilation conversion of infix expression to prefix and postfix expression, Tower of Hanoi problem, Representation of Queues, Operations on queues: Create, Add, Delete, Priority Queues, Dequeues, Circular Queue.

UNIT II

Linked Lists: Singly linked lists: Representation of linked lists in memory, Traversing, Searching, Insertion into, Deletion from linked list, Polynomial Addition, Header Linked List, Doubly linked list, generalized list.

UNIT III

Trees: Basic Terminology, Binary Trees and their representation, expression evaluation, Complete Binary trees, Extended binary trees, Traversing binary trees, Searching, Insertion and Deletion in binary search trees(with and without recursion), AVL trees, Threaded trees, B trees.
Graphs: Terminology and Representations, Graphs &Multigraphs, Directed Graphs, Sequential representation of graphs, Adjacency matrices, Transversal Connected Component and Spanning trees, Shortest path

UNIT IV

Searching, Sorting methodologies: Array- Bubble sort, Selection Sort, Insertion Sort, Linear Search, Binary Search. Stack -Quick Sort, Merge Sort. Two way Merge Sort. Queue- Radix Sort.Tree – Heap Sort.

Reference Books:

1. An introduction to data structures and application by Jean Paul Tremblay & Pal G. Sorenson (McGraw Hill)
2. R.L. Kruse, B.P. Leary, C.L. Tondo, Data structure and program design in C , PHI
3. R. B. Patel, Expert Data Structures With C, Khanna Publications, Delhi, India, 3rd Edition 2008.
4. Data Structures using C by A. M. Tenenbaum, Langsam, Moshe J. Augentem, PHI Pub.
5. Data Structures and Algorithms by A. V. Aho, J. E. Hopcroft and T. D. Ullman, Original edition, Addison-Wesley, 1999, Low Price Edition.
6. Fundamentals of Data Structure by Ellis Horowitz &SartajSahni, Pub, 1983. AW
7. Data Structure and Program design in C by Robert Kruse, PHI
8. Theory and Problems of Data Structures by Jr. SymourLipschetz, Schaum's outline by TMH.
9. Introduction to Computer Science- An algorithms approach, Jean Paul Tremblay, Richard B. Bunt, 2002, TMH.
10. Data Structure and Standard Template Library- Willam J. Collins, 2003, T.M.H

NOTE:

In the Semester examination, the examiner will set 08 questions in all selecting two from each unit. The candidates will be required to attempt five questions in all, atleast one from each unit. All questions carry equal marks.

ECE221B **DIGITAL ELECTRONICS LAB**

B. Tech. Semester –III (EE, ECE, CSE, IC, EEE, common with BME, AEI in 4th Sem.)

L	T	P	Credits
-	-	2	1

Class Work	:	20 Marks
Practical	:	30 Marks
Total	:	50 Marks

Duration of Exam. : 3 Hrs.

LIST OF EXPERIMENTS:

1. Study of TTL gates –AND,OR,NOT,NAND,NOR,EX-OR,EX-NOR
2. To realize the universal property of NAND gate
3. To realize the universal property of NOR gate
4. Design & realize a given function using K-maps and verify its performance.
5. To verify the operation of Multiplexer & De-multiplexer.
6. To verify the operation of Comparators.
7. To perform Half adder and Full adder
8. To perform Half Substractor and Full substractor.
9. To verify the truth table of S-R,J-K,T & D Type flip flop .
10. To verify the operation of bi-directional shift register.
11. To study analog to digital and digital to analog converter
12. To design & verify the operation of 3 bit synchronous counter.
13. To design & verify the operation of synchronous UP/DOWN decade counter using JK flip flop & derive a seven segment display using the same.
14. To design & verify the operation of asynchronous UP/DOWN decade counter using JK flip flop & derive a seven segmen ment display using the same.
15. Design a 4- bit shift register ,verify its operation and verify the operation of a ring counter and a Johnson counter.

Note:-

1. Total ten experiments are to be performed in the semester.
2. At least seven experiments should be performed from the above list. Remaining three experiments should be performed as designed and set by the concerned institution as per the scope of the syllabus.

Approved by UG BOS & FET

ECE223B **ANALOG ELECTRONICS LAB**

B. Tech. Semester –III (BME, ECE,common with 4th Sem. AEI)

L	T	P	Credits
-	-	2	1

Class Work	:	20 Marks
Practical	:	30 Marks
Total	:	50 Marks

Duration of Exam. : 3 Hrs.

LIST OF EXPERIMENTS:

1. Study of half wave and full wave rectifiers
2. Study of power supply filter.
3. Study of diode as a clipper and clamper.
4. Study of zener diode as a voltage regulator.
5. Study of CE amplifier for voltage,current and Power gains input,output impedances.
6. Study of CC amplifier as a buffer.
7. To study the frequency response of RC coupled amplifier.
8. Study of transistor as a constant current source in CE configuration .
9. To study characteristics of FET.
10. Study of FET common source amplifier.
11. Study of FET common drain amplifier.
12. Graphical determination of small signal hybrid parameter of bipolar junction transistor.
13. Study and design of a DC voltage doubler.

Note:-

1. Total ten experiments are to be performed in the semester.
2. At least seven experiments should be performed from the above list. Remaining three experiments should be performed as designed and set by the concerned institution as per the scope of the syllabus.

Approved by UG BOS & FET

EE241B **NETWORK ANALYSIS & SYNTHESIS LAB**

B. Tech. Semester –III (ECE, AEI)

L	T	P	Credits
-	-	2	1

Class Work	:	20 Marks
Practical	:	30 Marks
Total	:	50 Marks

Duration of Exam. : 3 Hrs.

LIST OF EXPERIMENTS:

1. Transient response of RC circuit.
2. Transient response of RL circuit.
3. To find the resonance frequency and Band width of RLC series circuit.
4. To calculate and verify "Z" parameters of a two port network.
5. To calculate and verify "Y" parameters of a two port network.
6. To determine equivalent parameter of parallel connections of two port network.
7. To plot the frequency response of low pass filter and determine half-power frequency.
8. To plot the frequency response of high pass filter and determine the half-power frequency.
9. To plot the frequency response of band-pass filter and determine the band-width.
10. To calculate and verify "ABCD" parameters of a two port network.
11. To synthesize a network of a given network function and verify its response.
12. Introduction of P-Spice.

Note:-

1 Total ten experiments are to be performed in the semester.

2 At least seven experiments should be performed from the above list. Remaining three experiments should be performed as designed and set by the concerned institution as per the scope of the syllabus.

CSE221B **DATA STRUCTURES LAB**

B. Tech. Semester –III (CSE, ECE,AEI)

L	T	P	Credits
-	-	2	1

Class Work	:	20 Marks
Practical	:	30 Marks
Total	:	50 Marks

Duration of Exam. : 3 Hrs.

LIST OF EXPERIMENTS:

Experimental work will be based upon the course Data Structures (CSE201B).

Note:-

1 Total ten experiments are to be performed in the semester.

ME217B **WORKSHOP TRAINING**

B. Tech. Semester –III (Common for all branches except BT & AE)

L	T	P	Credits
-	-	-	2

Class Work	:	50 Marks
Practical	:	-
Total	:	50 Marks

Each student has to undergo a workshop atleast 4 weeks (80-100 hours) at the end of II semester during summer vacations. **Out of the four weeks, two weeks would be dedicated to general skills and two weeks training for specialized discipline/department.** The evaluation of this training shall be carried out in the III semester

LIST OF JOBS TO BE CARRIED OUT DURING THIS PERIOD

1. To study and prepare different types of jobs on machine tools (lathe, shaper, planer, slotter, milling, drilling machines).
2. To prepare lay out on a metal sheet by making and prepare rectangular tray, pipe shaped components e.g. funnel.
3. To prepare joints for welding suitable for butt welding and lap welding.
4. To study various types of carpentry tools and prepare simple types of wooden joints.
5. To prepare simple engineering components/ shapes by forging.
6. To prepare mold and core assembly, to put metal in the mold and fettle the casting.
7. To study of CNC lathe, CNC Milling and EDM Machines.
8. Any work assigned in electrical workshop, computer hardware/language lab, electronics workshop, biomedical hardware, automobile workshop etc.

This student will prepare job(s)/project as an individual or in a group using workshop in house infrastructure.

The student shall submit a typed report.

Training will be evaluated on the spot out of 20 marks.

The report will be evaluated in the III Semester by a Committee consisting of two teachers.

The student will interact with the committee through presentation to demonstrate his/her learning. The basis of evaluation will primarily be the knowledge and exposure of students on different kinds of Machines/instruments/tools/skills etc. The committee will evaluate out of 30 marks.

The committee shall submit the awards out of 50 marks.